IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 10, October 2016

Design and Performance Analysis of different shapes of Trigate FinFET at 20nm

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Abstract: With the invention of new technology below 22nm, leakage current is increasing exponentially due to the different Short Channel Effects (SCEs). FinFETs have gain attractive attention due to their superior electrostatic control over channel and hence low SCEs. In this work, multigate FinFETs for gate length of 20nm for three different shapes viz. Rectangular, Trapezoidal and Triangular with different fin heights are designed using Cogenda TCAD (Technology Computer Aided Design) tool. It was observed that for any fin height of multigate FinFETs, the Triangular fin shape showed better improvement in the electrical characteristics in terms of Drain-Induced Barrier Lowering (DIBL); Threshold voltage roll off (V_t); Sub-threshold Swing (SS); Leakage current (I_{OFF}).The Rectangular trigate FinFET has very large leakage current which degrade its overall performance but it has maximum drive current (I_{ON}) as compare to other multigate FinFETs.

Keywords: FinFET; Drain-Induced Barrier Lowering; Threshold voltage roll off; Sub-threshold Swing; Leakage current, fin height, gate length.

I. INTRODUCTION

Downscaling of the CMOS technology has shifted to nanometer regime so as to achieve MOS integrated circuits with (i) high operational speed, and (ii) high compactness of packing. Because of exceptionally large integration, the power utilization of contemporary VLSI devices has turned out to be quite crucial [1]. Technology node has shrunk from 10 µm in 1971 to 90 nm in 2004 and will shrink to below 7 nm in 2020 [2]. In short channel MOSFETs, as length L of the channel is approaching to source depletion width and drain depletion width, therefore edge effects cannot be neglected, whereas in long channel MOSFETs dimensions of channel are of considerable length so that edge effects from all sides were not much significant and therefore neglected Fig. 1 shows the difference between the structures of long channel and short channel MOSFETs [4]. As the channel dimensions are lowered to take the advantage like area utilization by maximum components and lesser on-chip delay, various detrimental effects such as increase in Source-drain leakage current, increased gate tunneling current, large variations in device performance due to uncontrollable channel doping and enhancement of short channel effects in short channel MOSFETs like threshold voltage roll-off, drain-induced-barrier–lowering (DIBL), Punch- through, Channel length Modulation, Sub-threshold Swing, Leakage currents, Impact Ionization, Mobility Degradation, Velocity Saturation, Narrow Gate Width effects and Reverse Short channel effects emerges [5-7]. Multi-gate field-effect transistors such as fin-shaped FETs (FinFETs) have been considered as prominent device in place of conventional bulk planar transistors. FinFETs has better electrostatic control of the gate over the entire semiconductor channel, which results in an enhancement of on-current and a reduction of Short Channel Effects.

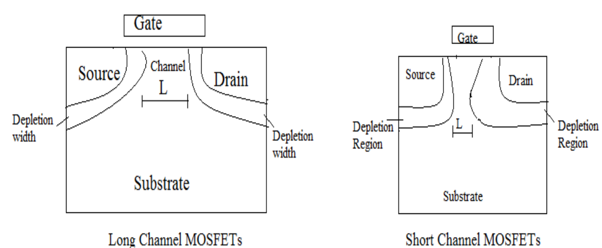

Fig. 1: Long channel and short channel MOSFETs [4]

II. LITERATURE SURVEY

Various design parameters of FinFET with 3-D numerical simulation and analytical modelling has been investigated and compared [8]. By using high doping concentration and corner with a small curvature radius, the value of parameters like I_{ON}/I_{OFF} ratio and the Subthreshold slope are degraded [9]. Non-uniform fin width and high fin height along vertical direction increase the SCEs because non-rectangular fin geometry leads to non-uniform current flow and current crowding in the vertical direction. DIBL and Subthreshold slope parameters was also greatly affected. Therefore, the choice of fin height has limited

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constraints for new designed device [10]. The limits for scaling in Double Gate underlap FinFET and Triple Gate overlap FinFET devices on the basis of gate-length, fin height and thickness using 2D and 3D simulators was investigated [11]. An unified FinFET compact model for complex fin dimensions which represent four different model parameters for analyses of device characteristics of different FinFETs structures was designed [12].

An analytical compact model for drain current of undoped and less doped nanoscale FinFET with Trapezoidal cross section was determined. The validation of results obtained from designed model was done by equating with 3-D numerical device simulations and it demonstrated very good accuracy for drain current and transcapacitances [13]. The impingement of the current flow shape in rectangular and tapered FinFETs on basis of threshold voltage variation induced by work-function variation by performing extensive 3-D TCAD simulations was demonstrated [14]. FinFET with triangular fin reduces leakage current by 70% over a FinFET with rectangular fin by taking the same width of fin. They have explored the application of different fin shape to multithreshold FinFET design. They have also described that using these techniques; it is possible to design ultralow-power n-FinFETs by maintaining high values of I_{ON}/I_{OFF}, threshold voltage, and subthreshold swing but with reduced leakage current [15].

In this work, three different shape of fins such as Rectangular, Trapezoidal, and Triangular with gate length of 20nm and gate oxide thickness 1nm for ten different fin heights of range 5nm, 10nm, 15nm, 20nm, 30nm, 40nm, 50nm, 60nm, 70nm, 80nm, for all multigate FinFETs using TCAD are implemented. The effect of different fin shapes and heights on device performance can be analysed in terms of V-I characteristics, Subthreshold swing (SS), Threshold voltage roll off (V_t) and drain induced barrier lowering (DIBL). The fin shape variation has been analysed mathematically and the performance of device have been studied in terms of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS, V_t and DIBL. At Last, the performance of Trigate Rectangular FinFET, Trapezoidal FinFET and Triangular FinFET have been compared for different process parameters. The rest of the paper has been organized as follows: Section III describes the device design & methodology. Section IV shows the results and discussions of the proposed work. Subsequent Section concludes the work done and conveys the future scope.

III.DEVICE DESIGN & METHODOLOGY

The Rectangular, Trapezoidal and Triangular Trigate FinFETs are designed using the following parameters: length of channel L=20nm; thickness of gate oxide t_{ox}= 1nm; doping concentration of the channel regions $N_A=10^{17}$ cm^{-3}; doping concentration of the source /drain contact regions $N_D= 10^{20}$ cm^{-3}; fin height H_{fin}= 5nm to 30nm; for Rectangular, top and bottom fin width W_{fin}=15nm; for Trapezoidal, bottom width of fin $W_{fin, bot}$=15nm; top width of fin $W_{fin, top}$= 10nm; for Triangular, bottom width of fin $W_{fin, bot}$=15nm; top width of fin $W_{fin, top}$= 0.001nm using Cogenda 3D TCAD numerical simulator tool.The 3D illustrations of the designed Rectangular, Trapezoidal and Triangular Trigate FinFET devices are shown in Fig. 2. Fig. 2. (a) shows the active region fin of the device which of rectangular, trapezoidal and triangular shape of height 30nm. Fig. 2. (b) shows the source pad, drain pad, active region, Tungsten metal gate and aluminium contacts. The Tungsten metal with work function 4.50eV for gate and metallic contact of aluminium was used for power supply. The active region was etched at height of 30 nm above the substrate. Finally, for the separation of different regions from each other the silicon dioxide was formed as shown in the Fig. 2. (c). Fig.2. (d) represents the Mesh size of FinFET structure. The designed FinFET Structures have been simulated using Cogenda TCAD numerical simulators.

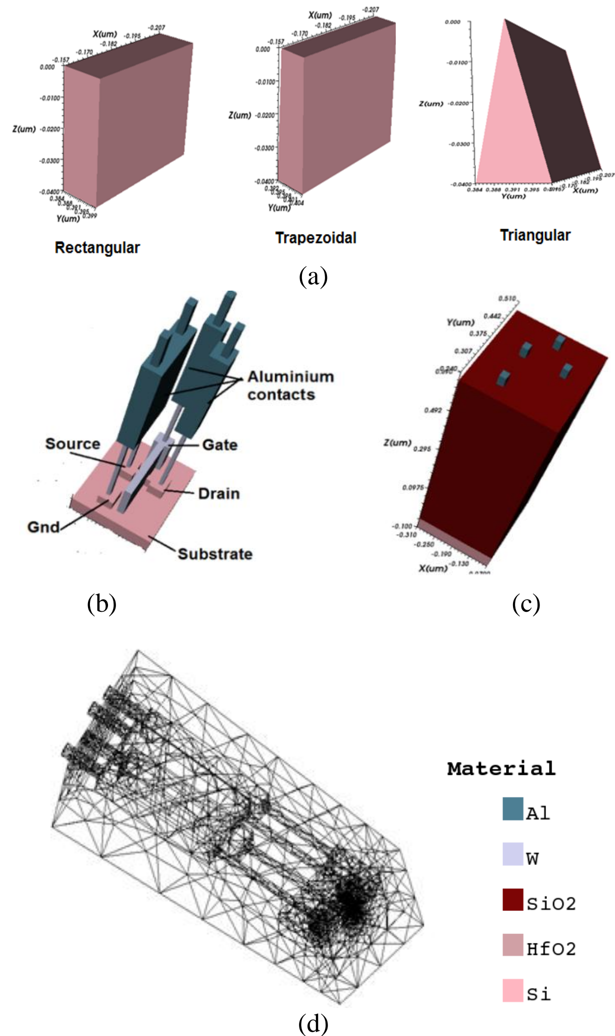

Fig 2 Bird's eye view of (a) Active region fin of Rectangular, Trapezoidal and Triangular shape of height 30nm, (b) Source pad, Drain pad, Active region, substrate,

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Tungsten gate and Metallic contact aluminium, (c) Formation of silicon dioxide which separate different regions from each other, (d) Mesh size of FinFET structure

The performance of designed Rectangular, Trapezoidal and Triangular Multigate FinFETs has been analysed using TCAD 3-D simulations using classical drift-diffusion approach and keeping external temperature 300K.

IV. SIMULATION SETUPS & RESULTS

The following performance parameters have been used for analysis of designed Rectangular, Trapezoidal and Triangular Multigate FinFET devices:-

i. **On Current (I_{ON}):** The on-current (I_{ON}) have been measured at gate voltage V_g = 1V and drain bias voltage of V_d =0.05V.

ii. **Off Current (I_{OFF}):** It indicates the leakage current of the device in off state. It have been measured at gate voltage V_g = 0V with the drain bias voltage of V_d = 0.05V.

iii. **I_{ON}/I_{OFF} Current ratio:** The I_{ON}/I_{OFF} ratio is measured as I_{ON} at V_g=1V and I_{OFF} at V_g=0V with drain bias voltage = 0.05.The switching performance of the device can be calculated using I_{ON}/I_{OFF}. Therefore, for better switching, high value of I_{ON}/I_{OFF} is required.

iv. **Subthreshold Swing (SS):** Subthreshold Swing is defined as the change in gate voltage per decade of drain voltage. It can be calculated directly using transfer characteristics by keeping drain current in logarithmic scale as shown in the eq.(1)

$$\text{Subthreshold swing (SS)} = \frac{dV_g)}{d\log(I_d)} \qquad \text{eq. (1)}$$

v. **Drain Induced Barrier Lowering (DIBL):** The DIBL is defined as the horizontal displacement of the transfer characteristics at constant drain current for drain voltage V_d= 0.02 and 1V.The constant drain current, I_C is given as [13].

$$I_C = \frac{W_{eff}}{L} \times 10^{-7} \qquad \text{eq. (2)}$$

where W_{eff} is Effective channel width and L is gate length. The effective channel width (W_{eff}) for Rectangular Trigate FinFET is [13]

$$W_{eff} = 2H_{fin} + W_{fin} \qquad \text{eq. (3)}$$

For Tapered Fin shape equivalent fin width $W_{fin,eq}$ is taken at its orthocentre

$$W_{fin} = W_{fin,eq}\, W_{fin,top} + \frac{\beta}{\beta+1}\left(W_{fin,bot} - W_{fin,top}\right) \text{eq. (4)}$$

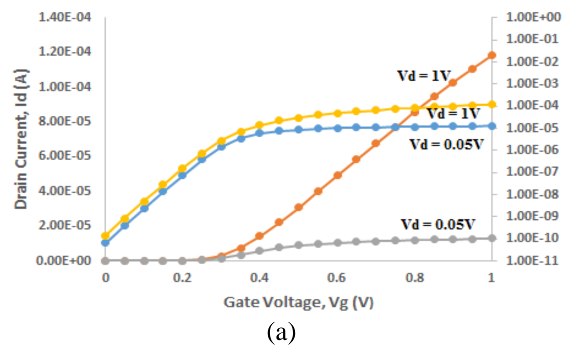
$$\text{where } \beta = \frac{2W_{fin,bot} + W_{fin,top}}{2W_{fin,top} + W_{fin,bot}} \qquad \text{eq. (5)}$$

vi. **Threshold Voltage Roll Off (V_t):** The threshold voltage roll off, (V_t) for all designed Multigate FinFETs have been measured directly from the transfer characteristics in the linear region with drain voltage V_d =0.05V using the maximum transconduction change method.

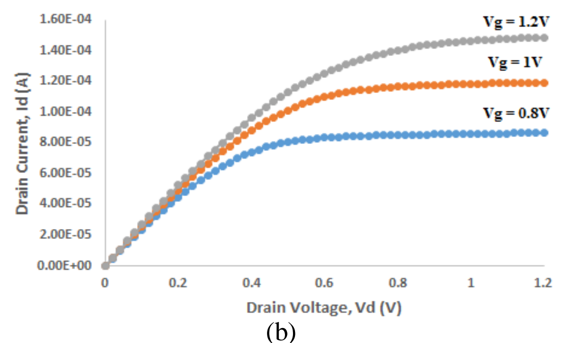
The simulated V-I characteristics of Rectangular, Trapezoidal and Triangular Multigate FinFET have been shown in the Fig. 3, Fig. 4 and Fig. 5 respectively. The transfer characteristics have been plotted for drain voltage of 50 mV and 1V in linear as well as in logarithmic scale and the output characteristics for different gate voltage ranging from 0.8 to 1.2V. The calculated electrical parameters based on the simulations result of 20nm Rectangular, Trapezoidal and Triangular FinFET for 10nm, 15nm and 30nm Fin Heights have been listed in the Table I.

Table I Electrical parameters based on the simulations result of 20nm rectangular, trapezoidal and triangular finfet for 10nm, 15nm and 30nm fin heights.

Fin Shape	Fin Height (nm)	Ion (A)	Ioff (A)	Ion/Ioff ratio	SS (mV/dec)	V_t (V)	DIBL (mV/V)
Rectangular	10	1.21E-05	3.92E-11	3.09E+05	66	0.258156	41
	15	1.29E-05	6.52E-11	1.98E+05	70	0.249191	45
	30	1.41E-05	1.14E-10	1.24E+05	66	0.233481	41
Trapeziodal	10	9.60E-06	2.62E-11	3.66E+05	66	0.253375	36
	15	1.15E-05	4.16E-11	2.76E+05	63	0.245083	40
	30	1.14E-05	7.53E-11	1.51E+05	60	0.228869	32
Triangular	10	5.82E-06	1.19E-11	4.88E+05	61	0.244839	24
	15	5.68E-06	1.47E-11	3.86E+05	60	0.242036	21
	30	5.03E-06	2.25E-11	2.23E+05	65	0.238227	36



(a)



(b)

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DOI 10.17148/IJIREEICE.2016.41015

IJIREEICE
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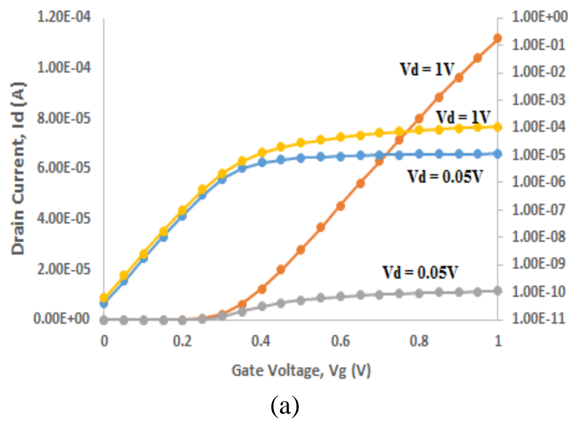
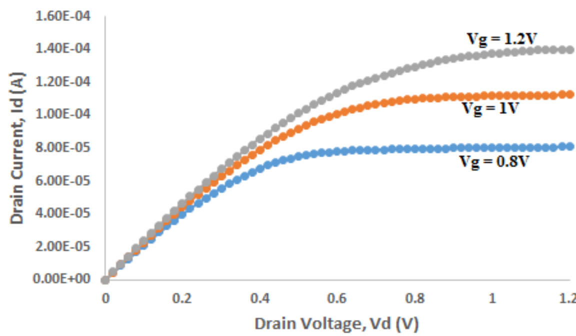
Electrical, Electronics, Instrumentation and Control Engineering
ISO 3297:2007 Certified
Vol. 4, Issue 10, October 2016

Fig.3. Simulated (a) Transfer characteristics in linear and logarithmic scales and (b) output characteristics of Trigate Rectangular FinFET for 20nm gate length

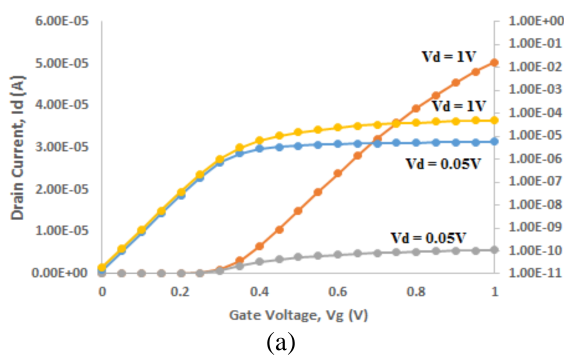


(a)

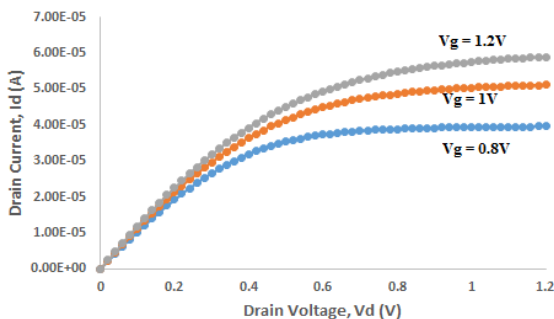


(b)

Fig. 4. Simulated (a) Transfer characteristics in linear and logarithmic scales and (b) output characteristics of Trigate Trapezoidal FinFET for 20nm gate length.



(a)



(b)

Fig. 5. Simulated (a) transfer characteristics in linear and logarithmic scales and (b) output characteristics of Trigate Triangular FinFET for 20nm gate length.

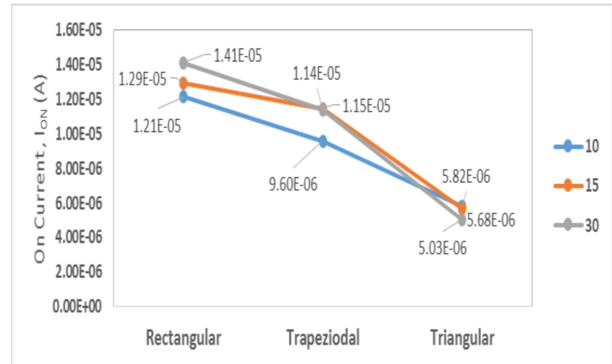


Fig. 6. On Current (I_{ON}) of 20nm Rectangular, Trapezoidal and Triangular FinFETs for different fin heights

Fig. 6 shows the impact of different fin height of 20nm Rectangular, Trapezoidal and Triangular FinFETs on I_{ON} parameter. Since the rectangular fin shape for all fin heights has maximum I_{ON} current because it has the maximum top fin width and bottom fin width of 15nm. Whereas triangular fin shape has minimum I_{ON} current as its top fin width varies in the range of 15nm to 0nm as we move from bottom to the top. The fin shape like trapezoidal has mid-range of I_{ON} current in comparison with rectangular and triangular fin shape.

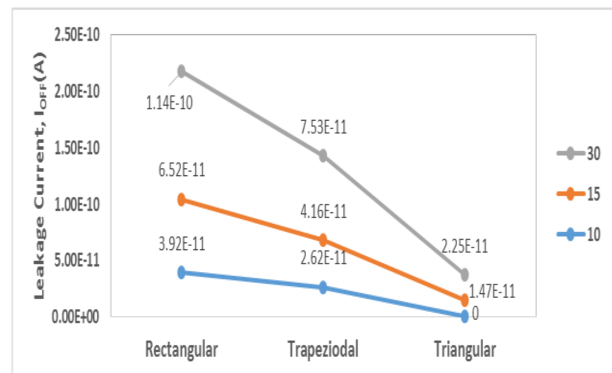


Fig.7. off Current (I_{OFF}) of 20nm Rectangular, Trapezoidal and Triangular FinFETs for different fin heights

Fig. 7 shows the fin height analysis in terms of I_{OFF} for Rectangular, Trapezoidal and Triangular FinFETs. It was observed that the due to thin top fin width Triangular FinFET has lower off current as compared with Rectangular and Trapezoidal.

In this case, due to lesser fin width the gate allow to almost shut off the current flow in the off state thus reducing the I_{OFF}. But in Rectangular fin shape, the off current is high due to thick fin width because thick width leads to reduction in gate controllability of the channel thus forming the leakage path in the region which is far from gate terminal.

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DOI 10.17148/IJIREEICE.2016.41015

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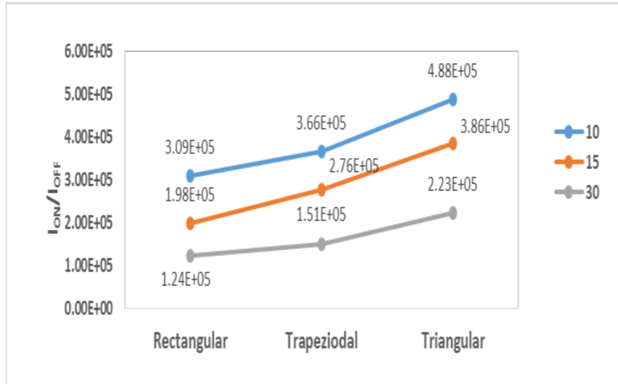

Fig. 8. I_{ON}/I_{OFF} of 20nm Rectangular, Trapezoidal and Triangular FinFETs for different fin heights

Fig. 8 indicates that the different fin height analysis in terms of I_{ON}/I_{OFF}. It was observed that the Triangular FinFET has low value of I_{OFF} current therefore; it has high I_{ON}/I_{OFF} for all fin heights as compared to Rectangular and Trapezoidal.

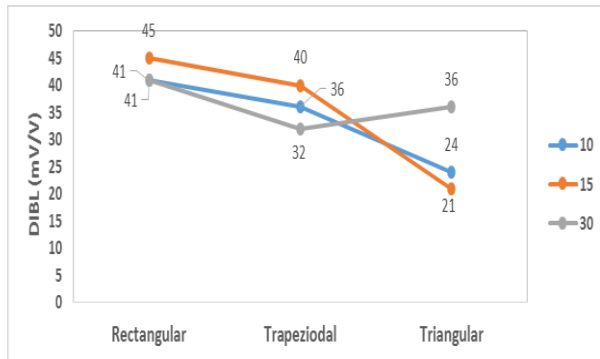

Fig. 9. DIBL of 20nm Rectangular, Trapezoidal and Triangular FinFETs for different fin heights

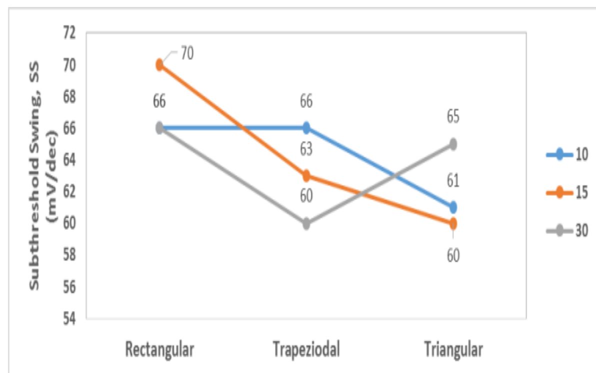

Fig. 10. Subthreshold Swing of 20nm Rectangular, Trapezoidal and Triangular FinFETs for different fin heights

Fig. 9 shows the fin height analysis in terms of DIBL for rectangular, trapezoidal and triangular FinFETs. It was observed that in Triangular and Trapezoidal have less effect of DIBL due to thin top fin width and better the gate controllability of the channel as compared to Rectangular FinFET.

Fig.10 shows that for all fin heights, the SS of Rectangular FinFET was in the range 60 to 70mV/dec. whereas for the Triangular and Trapezoidal fin shape was in the range of 60 to 66mV/dec due to better gate-to channel controllability in tapered.

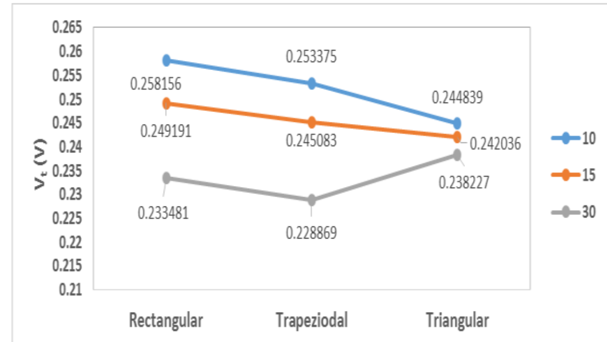

Fig. 11. Threshold Voltage Roll off of 20nm Rectangular, Trapezoidal and Triangular FinFETs for different fin heights

Fig.11 indicates the fin height analysis of 20nm Rectangular, Trapezoidal and Triangular FinFET in terms of V_t. The Triangular fin shape has less effect of V_t as compared with Rectangular and Trapezoidal.

V. CONCLUSION AND FUTURE WORK

Rectangular, Triangular and Trapezoidal Multigate FinFETs was designed and analyzed for gate length of 20nm. Their performance was analyzed in terms of Voltage-Current Characteristics and Short Channel Effects like Drain-Induced Barrier Lowering, Threshold Voltage Roll Off and Sub-threshold Swing. It was observed that for any fin height the Triangular fin shape can improved the electrical characteristics of multigate FinFETs**.** The Rectangular has very large leakage current which degrade its overall performance but it has maximum drive current (I_{ON}) as compare to other FinFETs.

In future the other fin shapes like pentagonal, hexagonal etc and the combination of two or more can be implemented for designing high performing multi-fin FinFETs. For getting improved SCE and drive current hybrid Triangular fin shape mixing with rectangular, pentagonal, irregular hexagonal can be designed.

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DOI 10.17148/IJIREEICE.2016.41015

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Electrical, Electronics, Instrumentation and Control Engineering
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